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EXAMINER	
ODOM, CURTIS B	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/498,893	GRONEMEYER, STEVEN A.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-9,11,12,14,15,17-23,26-29,39-42 and 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-9,11,12,14,15,17-23,26-29,39-42 and 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/26/2007 have been fully considered but they are not persuasive.

Applicant states the combination of Krasner (U. S. Patent No. 6, 289, 041) and Mendelovicz (U. S. Patent No. 6, 005, 903) fails to establish a prima facie case of obviousness. However, it is the understanding of the Examiner that the combination does in fact establish a prima facie case of obviousness.

First, all the limitations are taught or suggested by the prior art (see rejection below). Krasner further discloses the time domain signal processor of Fig. 4 is a matched filter processor in that it contains a matched filter (see Fig. 4, block 408), wherein the data period of the matched filter (time domain signal processor) is 20 PN frames (see column 6, lines 29-34), which is equivalent to 20 ms (see column 1, lines 28-38). It is the understanding of the Examiner that based on the specification, 20 ms time periods are equivalent to T20 periods (see instant specification page7, lines 8-18). Thus, it is the understanding of the Examiner that Krasner and Mendelovicz discloses all the claim limitations including a matched filter processor synchronized to a T20 period (20 ms period).

Second, Krasner provides motivation to combine the references since Krasner states that in order to build up the spikes (magnitudes) used to detect a correlation, a square-law or other

detection method (such as the square root of the sum of the squares disclosed by Mendelovicz) can be used to remove varying phase angles (column 4, lines 12-15).

Third, there is a reasonable expectation of success since both Krasner (see Fig. 4) and Mendelovicz (see Fig. 4) both disclose match filter processors for spread spectrum signals. Thus, based on the above disclosure, it is the understanding of the Examiner that the combination does in fact establish a prima facie case of obviousness.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5, 8, 9, 11, 14, 15, 20, 22, 23, 26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krasner (previously cited in Office Action 4/21/2005) and in view of Mendelovicz (previously cited in Office Action 7/26/2006).

Regarding claim 1, Krasner discloses a system (Fig. 4) for processing communication data from a code signal input (PN signal), the system comprising:

a signal sampler (not shown) operable to receive digital GPS signals to produce original samples at 2 samples per chip as described in column 5, line 66-column 6, lines 16;

a Doppler shift system comprising of a microcontroller (Fig. 4, blocks 428) to provide Doppler sample time and Doppler frequency shift correction values as described in column 5, lines 28-50 and shown in Fig. 4 ;

a register bank (Fig. 4, block 418, column 7, lines 58-61) representing a storage circuit to received and store signal data;

a time domain signal processor (Fig. 4, blocks 404, 408, 410, 416, 420, 426) comprising:

a digital frequency translation circuit (Fig. 4, block 404) representing a complex mixer, coupled to the register band and Doppler shift system, for multiplying (mixing) the input signal with the Doppler frequency offset correction value (see column 5, lines 28-50) from the microcontroller;

a PN matched filter (Fig. 4, block 408) representing a complex product generation circuit, coupled to the frequency translation circuit and a PN code signal input from the microcontroller, which computes a complex product by multiplying the mixed portion (frequency translated) portion of the signal data with a current PN code phase of a PN code signal (see column 3, lines 28-40, wherein the input signal are multiplied by the current PN code phase (chip) in a matched filter to generate a spike (complex number) as described in column 3, lines 64-column 4, line 5)

a predetection loop integrator (Fig. 4, block 410, column 6, lines 29-45) which sums the complex numbers (spikes) for 20 PN frames (see also column 4, lines 15-25) to generate a coherent integration value;

a magnitude squaring circuit (Fig. 4, block 416) for performing a magnitude square-law operation (see column 5, lines 6-14) of the coherent integration values to obtain a magnitude value;

a post detection loop integrator (Fig. 4, block 420) for processing the magnitude-squared values output from the magnitude squaring circuit as described in column 6, lines 29-45, and

wherein the time domain signal processor is in signal communication with the signal sampler, the Doppler shift system and the code signal input, the time domain signal processor operable to shift the signal data by a Doppler frequency offset correction value (see column 5, lines 37-50, wherein the multiplication frequency shifts signal data) and to determine a correlation in the matched filter between the shifted signal (output from the frequency translation circuit) and the code signal input (PN signal) as described in column 3, lines 29-39, where the code phase (chip) and the computed magnitude having the largest magnitude (spike) indicates a match (correlation) between the transmitted (shifted) waveform) and the PN code signal (see column 3, lines 64-column 4, line 3) and wherein the time domain signal processor is a matched filter processor in that it contains a matched filter (see Fig. 4, block 408), wherein the data period of the matched filter (time domain signal processor) is 20 PN frames (see column 6, lines 29-34), which is equivalent to 20 ms (see column 1, lines 28-38). It is the understanding of the Examiner that based on the specification, 20 ms time periods are equivalent to T20 periods (see instant specification page7, lines 8-18).

Krasner does not disclose the magnitude squaring circuit comprises a square root circuit for computing a square root value of the sum of the sum of the squares of the coherent integration values, each square root having a magnitude and associated phase.

However, Mendelovicz discloses a matched filter correlator (Fig. 4), similar to that of Krasner, which acquires a signal wherein each code (phase) (SSC) modified by Doppler is correlated against each time of arrival (input signal) until a match is found which allows

acquisition of the signal (column 6, lines 53-60). The output of the correlator is supplied to a magnitude computation circuit (Fig. 4, block 47) which computes a magnitude and phase of the correlation products (column 11, lines 31-33) by taking a square root value of the sum of the sum of the squares of the correlation values (see column 2, lines 6-9). The largest magnitude values are then used to indicate correlation (acquisition) between the code (SSC) and the data word (input signal), see column 11, lines 33-41. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the system of Krasner to generate a magnitude value using the square root of the sum of the squares as taught by Mendelovicz rather than magnitude-squaring since Krasner states that in order to build up the spikes (magnitudes) used to detect a correlation, a square-law or other detection method (such as the square root of the sum of the squares disclosed by Mendelovicz) can be used to remove varying phase angles (column 4, lines 12-15).

Regarding claim 2, Krasner discloses a GPS signal acquired using a PN code input signal (column 3, lines 26-40) wherein the signals are direct sequence spread spectrum signals (column 1, lines 20-24), wherein acquiring the different GPS signals using the PN code signals (column 1, lines 30-38) is "direct sequence" CDMA processing.

Regarding claim 5, Krasner discloses the Doppler shift system further comprises a microcontroller (Fig. 4, block 428) which generates a Doppler shift represented by a Doppler frequency offset (column 5, lines 28-50), to compensate for Doppler shifts (offsets) in the received signal.

Regarding claim 8, Krasner discloses receiving (column 3, lines 28-30) and sampling (column 5, line 66-column 6, line 8) GPS signals, wherein GPS signals are radio frequency signals.

Regarding claim 9, Krasner discloses a method for processing communication data from comprising:

receiving (column 9, lines 31-35) GPS signal data

applying a Doppler frequency shift correction value using a digital frequency translation circuit (Fig. 4, block 404) which multiplies (mixes) the input signal with the Doppler frequency offset (shift) correction value (column 5, lines 28-50) from the microcontroller as results in a Doppler frequency shifted signal;

receiving a PN code signal at PN matched filter (see Fig. 4, block 408) from microcontroller (Fig. 4, block 428);

determining a correlation (match) between the Doppler shifted signals and the PN code signal in a time domain using a PN matched filter (Fig. 4, block 408) as described in column 3, lines 63-67, wherein the data period of the matched filter (time domain signal processor) is 20 PN frames (see column 6, lines 29-34), which is equivalent to 20 ms (see column 1, lines 28-38, it is the understanding of the Examiner that based on the specification, 20 ms time periods are equivalent to T20 periods, see instant specification page7, lines 8-18) that further includes,

computing complex products by multiplying the mixed portion (frequency translated) portion of the signal data with a current PN code phase of a PN code signal (see column 3, lines 28-40, wherein the input signal are multiplied by the current PN code phase (chip) in a matched filter to generate a spike (complex number) as described in column 3, lines 64-column 4, line 5)

summing (Fig. 4, block 410, column 6, lines 29-45) the complex numbers (spikes) for 20 PN frames (see also column 4, lines 15-25) to generate a coherent integration value;

generating a magnitude value (Fig. 4, block 416) by performing a magnitude square-law operation (see column 5, lines 6-14) of the coherent integration values to obtain a magnitude value;

shifting the PN code signal to a next code chip (phase) one time offset at a time (see column 3, lines 33-39)

repeating the above steps for all of the seven code chips (phases) of the frames (see column 3, lines 33-39 and column 4, lines 58-62),where the code phase (chip) and the computed magnitude having the largest magnitude (spike) indicates a match (correlation) between the transmitted (shifted) waveform) and the PN code signal (see column 3, lines 64-column 4, line 3)

Krasner does not disclose generating a magnitude comprises computing a square root value of the sum of the sum of the squares of the coherent integration values, each square root having a magnitude and associated phase.

However, Mendelovicz discloses a matched filter correlator (Fig. 4), similar to that of Krasner, which acquires a signal wherein each code (phase) (SSC) modified by Doppler is correlated against each time of arrival (input signal) until a match is found which allows acquisition of the signal (column 6, lines 53-60). The output of the correlator is supplied to a magnitude computation circuit (Fig. 4, block 47) which compute a magnitude and phase of the correlation products (column 11, lines 31-33) by taking a square root value of the sum of the sum of the squares of the correlation values (see column 2, lines 6-9). The largest magnitude values are then used to indicate correlation (acquisition) between the code (SSC) and the data word

(input signal), see column 11, lines 33-41. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Krasner to generate a magnitude value using the square root of the sum of the squares as taught by Mendelovicz rather than magnitude-squaring since Krasner states that in order to build up the spikes (magnitudes) used to detect a correlation, a square-law or other detection method (such as the square root of the sum of the squares disclosed by Mendelovicz) can be used to remove varying phase angles (column 4, lines 12-15).

Regarding claim 11, Krasner discloses receiving a Doppler frequency offset (shift) correction value (column 5, lines 28-50) from a microcontroller (Fig. 4, block 428).

Regarding claim 14, Krasner discloses determining the correlation (match) using a matched filter (column 3, lines 55-67).

Regarding claim 15, Krasner discloses a system (Fig. 4) for processing GPS radio frequency data comprising:

a signal sampler (not shown) operable to receive digital GPS signals to produce original samples at 2 samples per chip as described in column 5, line 66-column 6, lines 16;

a Doppler shift corrector comprising of a microcontroller (Fig. 4, block 428) to provide Doppler sample time and Doppler frequency shift correction values as described in column 4, lines 28-50 and shown in Fig. 4 ;

a PN matched filter (Fig. 4, block 408) operable to receive a PN code signal;

a time domain signal processor (Fig. 4, blocks 404, 408, 410, 416, 420, 426) coupled to the signal sampler, the Doppler shift corrector and the code signal receiver, the time domain signal processor operable to shift the signal data by a Doppler frequency offset correction value

(see column 5, lines 37-50, wherein the multiplication shifts signal data) and to determine a correlation in the matched filter between the shifted signal (output from the frequency translation circuit) and the code signal input (PN signal) as described in column 3, lines 29-39, wherein the data period of the matched filter (time domain signal processor) is 20 PN frames (see column 6, lines 29-34), which is equivalent to 20 ms (see column 1, lines 28-38, it is the understanding of the Examiner that based on the specification, 20 ms time periods are equivalent to T20 periods, see instant specification page7, lines 8-18) and further includes,

a digital frequency translation circuit (Fig. 4, block 404) representing a complex mixer, coupled to the signal sampler, for multiplying (mixing) the input signal with the Doppler frequency offset correction value (column 5, lines 28-50) from the microcontroller;

a PN matched filter (Fig. 4, block 408) representing a complex product processor coupled to the frequency translation circuit and a PN code signal input from the microcontroller, which computes a complex product by multiplying the mixed portion (frequency translated) portion of the signal data with a current PN code phase of a PN code signal (see column 3, lines 28-40, wherein the input signal are multiplied by the current PN code phase (chip) in a matched filter to generate a spike (complex number) as described in column 3, lines 64-column 4, line 5)

a predetection loop integrator (Fig. 4, block 410, column 6, lines 29-45) which sums the complex numbers (spikes) for 20 PN frames (see also column 4, lines 15-25) to generate a coherent integration value;

a magnitude squaring circuit (Fig. 4, block 416) for performing a magnitude square-law operation (see column 5, lines 6-14) of the coherent integration values to obtain a magnitude value;

a controller to determine the code phase (chip) and the computed magnitude having the largest magnitude (spike) as compared to a threshold (see column 5, lines 14-27) indicating a match (correlation) between the transmitted (shifted) waveform) and the PN code signal (see column 3, lines 64-column 4, line 3);and

a demodulator (Fig. 9, block 400b) representing a signal processor coupled to the signal sample receiver (of the acquisition circuit 400a), the signal processor operable to process the signal data to extract encoded (modulated) data (column 13, lines 41-43).

Krasner does not disclose the magnitude squaring circuit comprises a square root processor for computing a square root value of the sum of the sum of the squares of the coherent integration values, each square root having a magnitude and associated phase.

However, Mendelovicz discloses a matched filter correlator (Fig. 4), similar to that of Krasner, which acquires a signal wherein each code (phase) (SSC) modified by Doppler is correlated against each time of arrival (input signal) until a match is found which allows acquisition of the signal (column 6, lines 53-60). The output of the correlator is supplied to a magnitude computation circuit (Fig. 4, block 47) which compute a magnitude and phase of the correlation products (column 11, lines 31-33) by taking a square root value of the sum of the sum of the squares of the correlation values (see column 2, lines 6-9). The largest magnitude values are then used to indicate correlation (acquisition) between the code (SSC) and the data word (input signal), see column 11, lines 33-41. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the system of Krasner to generate a magnitude value using the square root of the sum of the squares as taught by Mendelovicz rather than magnitude-squaring since Krasner states that in order to build up the spikes (magnitudes)

used to detect a correlation, a square-law or other detection method (such as the square root of the sum of the squares disclosed by Mendelovicz) can be used to remove varying phase angles (column 4, lines 12-15).

Regarding claim 20, Kranser discloses the processor is a time domain signal processor (column 3, lines 33-41, wherein comparing the received signal to the PN code signal one **time offset** at a time makes the processor of Krasner a time domain signal processor).

Regarding claim 22, Krasner discloses a system (Fig. 4) for processing communication data from a code signal input (PN signal), the system comprising:

a signal sampler (not shown) operable to receive digital GPS signals to produce original samples at 2 samples per chip as described in column 5, line 66-column 6, lines 16;

a Doppler shift corrector comprising of a microcontroller (Fig. 4, block 428) to provide Doppler sample time and Doppler frequency shift correction values as described in column 5, lines 28-50) and shown in Fig. 4 ;

a time domain signal processor (Fig. 4, blocks 404, 408, 410, 416, 420, 426) coupled to the signal sampler, the Doppler shift corrector and the code signal receiver, the time domain signal processor operable to shift the signal data by a Doppler frequency offset correction value (see column 5, lines 37-50, wherein the multiplication shifts signal data) and to determine a correlation in the matched filter between the shifted signal (output from the frequency translation circuit) and the code signal input (PN signal) as described in column 3, lines 29-39, wherein the time domain signal processor is a matched filter processor in that it contains a matched filter (see Fig. 4, block 408), wherein the data period of the matched filter (time domain signal processor) is 20 PN frames (see column 6, lines 29-34), which is equivalent to 20 ms (see column 1, lines

28-38, it is the understanding of the Examiner that based on the specification, 20 ms time periods are equivalent to T20 periods, see instant specification page7, lines 8-18) and further includes,

a register bank representing a means for storing (Fig. 4, block 418, column 7, lines 58-61) to receive and store signal data;

a digital frequency translation circuit representing a means for complex mixing (Fig. 4, block 404) coupled to the register bank and Doppler shift controller, for multiplying (mixing) the input signal with the Doppler frequency offset correction value (column 5, lines 28-50) from the microcontroller;

a PN matched filter representing a means for complex product generation (Fig. 4, block 408) coupled to the frequency translation circuit and a PN code signal input from the microcontroller, which computes a complex product by multiplying the mixed portion (frequency translated) portion of the signal data with a current PN code phase of a PN code signal (see column 3, lines 28-40, wherein the input signals are multiplied by the current PN code phase (chip) in a matched filter to generate a spike (complex number) as described in column 3, lines 64-column 4, line 5);

a predetection loop integrator representing a means for summing (Fig. 4, block 410, column 6, lines 29-45) which sums the complex numbers (spikes) for 20 PN frames (see also column 4, lines 15-25) to generate a coherent integration value;

a magnitude squaring circuit representing a means for generating a magnitude envelope (Fig. 4, block 416) for performing a magnitude square-law operation (see column 5, lines 6-14) of the coherent integration values to obtain a magnitude envelope value;

a controller representing an output processing circuit to determine the code phase (chip) and the computed magnitude having the largest magnitude (spike) as compared to a threshold (see column 5, lines 14-27) indicating a match (correlation) between the transmitted (shifted) waveform) and the PN code signal (see column 3, lines 64-column 4, line 3);and

Krasner does not disclose the magnitude squaring circuit (means for generating a magnitude envelope) comprises computing a square root value of the sum of the sum of the squares of the coherent integration values, each square root having a magnitude and associated phase.

However, Mendelovicz discloses a matched filter correlator (Fig. 4), similar to that of Krasner, which acquires a signal wherein each code (phase) (SSC) modified by Doppler is correlated against each time of arrival (input signal) until a match is found which allows acquisition of the signal (column 6, lines 53-60). The output of the correlator is supplied to a magnitude computation circuit (Fig. 4, block 47) which compute a magnitude and phase of the correlation products (column 11, lines 31-33) by taking a square root value of the sum of the sum of the squares of the correlation values (see column 2, lines 6-9). The largest magnitude values are then used to indicate correlation (acquisition) between the code (SSC) and the data word (input signal), see column 11, lines 33-41. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the system of Krasner to generate a magnitude value using the square root of the sum of the squares as taught by Mendelovicz rather than magnitude-squaring since Krasner states that in order to build up the spikes (magnitudes) used to detect a correlation, a square-law or other detection method (such as the square root of

the sum of the squares disclosed by Mendelovicz) can be used to remove varying phase angles (column 4, lines 12-15).

Regarding claim 23, Krasner discloses a GPS signal acquired using a PN code input signal (column 3, lines 26-40) wherein the signals are direct sequence spread spectrum signals (column 1, lines 20-24), wherein acquiring the different GPS signals using the PN code signals (column 1, lines 30-38) is "direct sequence" CDMA processing.

Regarding claim 26, Krasner discloses the Doppler shift system further comprises a microcontroller (Fig. 4, block 428) which generates a Doppler shift represented by a Doppler frequency offset (column 5, lines 28-50), to compensate for Doppler shifts (offsets) in the received signal.

Regarding claim 29, Krasner discloses receiving (column 3, lines 28-30) and sampling (column 5, line 66-column 6, line 8) GPS signals, wherein GPS signals are radio frequency signals.

4. Claims 6, 12, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Krasner (previously cited in Office Action 4/21/2005) and in view of Mendelovicz (previously cited in Office Action 7/26/2006) as applied to claims 1, 9, and 22, and in further view of Furukawa et al. (previously cited in Office Action 7/26/2006).

Regarding claim 6, Krasner and Menelovicz do not disclose a lookup table comprising stored precomputed Doppler shift correction values.

However, Furukawa et al. discloses a coherent detection system which stores precomputed correction values (passbands) which compensate for Doppler shifts related to an input signal (see column 2, lines 50-63). The filter settings (passbands) are selected based on the

Doppler shift in the signal. Therefore, it would have been obvious to store precomputed correction values in the system of Krasner and Mendelovicz as taught by Furukawa et al. since Furukawa et al. states implementing these teachings can allow for demodulation of a signal even when a large Doppler shift occurs (column 2, lines 2-4).

Regarding claim 12, Krasner and Menelovicz disclose multiplying (mixing) the input signal with the Doppler frequency offset correction value (see Krasner, column 5, lines 28-50) from the microcontroller. Krasner and Menelovicz do not disclose receiving the Doppler shift correction value from a lookup table.

However, Furukawa et al. discloses a coherent detection system which stores precomputed correction values (passbands) which compensate for Doppler shifts related to an input signal (see column 2, lines 50-63). The filter settings (passbands) are selected based on the Doppler shift in the signal. Therefore, it would have been obvious to store precomputed correction values in a lookup table in the system of Krasner and Mendelovicz as taught by Furukawa et al. since Furukawa et al. states implementing these teachings can allow for demodulation of a signal even when a large Doppler shift occurs (column 2, lines 2-4).

Regarding claim 27, the claimed system includes similar limitations corresponding to the above rejection of claim 6, which is applicable hereto.

5. Claims 7 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krasner (previously cited in Office Action 4/21/2005) and in view of Mendelovicz (previously cited in Office Action 7/26/2006) as applied to claims 1, 9, and 22, and in further view of Koenck et al. (previously cited in Office Action 7/26/2006).

Regarding claims 7 and 28, Krasner and Mendelovicz do not disclose the Doppler shift system or microcontroller (providing means) is coupled to the time domain signal processor by a data bus.

However, Koenck et al. discloses a high speed communication bus (Fig. 2, element 50) used to communication data between various modules in a data processing terminal (see column 15, lines 28-35). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to communicate data from the Doppler shift system/microcontroller to the time domain signal processor of Krasner and Mendelovicz using a high-speed bus as disclosed by Koenck since Koenck states the high-speed bus (MBUS) provides reliability advantages (column 15, lines 28-35) and more compact physical routing of the cables between the modules (column 17, lines 42-44).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krasner (previously cited in Office Action 4/21/2005) and in view of Mendelovicz (previously cited in Office Action 7/26/2006) as applied to claims 15, and in further view of Nossen (previously cited in Office Action 7/26/2006).

Regarding claim 21, Krasner and Mendelovicz do not disclose the processor used to determined a correlation between the code signal and the Doppler shifted data is a frequency domain processor.

However, Nossen discloses performing matched filter correlation techniques similar to that of Krasner and Mendelovicz in the frequency domain (column 1, lines 55-61), wherein a Doppler shifted signal (column 1, lines 35-43) is compared with a code (PRS) signal to determine the largest correlation pulse between the signal and the code which represents signal

acquisition (see column 1, lines 45-54). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to implement the processor of Krasner and Mendelovicz as a matched filter frequency domain processor disclosed by Nossen to reduce signal acquisition (searching) time (see Nossen, column 1, lines 52-61).

7. Claims 17-19, 39, 40 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krasner (previously cited in Office Action 4/21/2005) and in view of Mendelovicz (previously cited in Office Action 7/26/2006) as applied to claims 9 and 15, and in further view of Warren et al. (previously cited in Office Action 7/26/2006).

Regarding claims 17-19, Krasner and Mendelovicz do not disclose the system is implemented in computer code operating on a computer processor of CDMA radio receiver, or the system implemented on in a semiconductor device or application-specific integrated circuit (ASIC).

However, Warren et al. discloses a direct sequence spread spectrum radio receiver (Fig. 3, column 2, lines 38-45, wherein CDMA is a direct sequence spread spectrum signal) comprising a matched filter (Fig. 3, block 26) used to correlate the received signal with a code sequence to acquire the original transmitted signal (column 4, lines 26-39). Warren also discloses the receiver can be implemented as a semiconductor device, ASIC, software (computer code) or firmware (see column 6, lines 20-36). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the system of Krasner and Mendelovicz to allow the system to be implemented as a semiconductor device, ASIC, or software to increase the adaptability of the system by allowing various adaptations (see Warren et al., column 6, lines 20-23).

Regarding claim 39 and 40, Krasner and Mendelovicz disclose all the limitations of claims 39 and 40 (see above rejection of claim 9) including complex multiplying (mixing) the input signal with the Doppler frequency offset (shift) correction value (see Krasner, column 5, lines 28-50). Krasner and Mendelovicz do not disclose the method of claim 9 written as software in a computer readable medium.

However, Warren et al. discloses a direct sequence spread spectrum radio receiver/method (Fig. 3, column 2, lines 38-45, wherein CDMA is a direct sequence spread spectrum signal) comprising a matched filter (Fig. 3, block 26) used to correlate the received signal with a code sequence to acquire the original transmitted signal (column 4, lines 26-39). Warren also discloses the receiver/method can be implemented as a semiconductor device, ASIC, software (computer code) or firmware (see column 6, lines 20-36). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the method of Krasner and Mendelovicz to allow the system to be implemented as a semiconductor device, a computer readable medium such as an ASIC, or software to increase the adaptability of the system by allowing various adaptations (see Warren et al., column 6, lines 20-23).

Regarding claim 44, Krasner et al. further discloses processing the Doppler (frequency translatied) shifted data and PN code signal using a matched filter (Fig. 1, block 408)

8. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krasner (previously cited in Office Action 4/21/2005) and in view of Mendelovicz (previously cited in Office Action 7/26/2006) and in further view of Warren et al. (previously cited in Office Action 7/26/2006) as applied to claim 39, and in further view of Koenck et al. (previously cited in Office Action 7/26/2006).

Regarding claim 41, Krasner, Mendelovicz, and Warren et al. disclose all the limitations of claim 41 including complex multiplying (mixing) the input signal with the Doppler frequency offset (shift) correction value (see Krasner, column 5, lines 28-50). Krasner, Mendelovicz, and Warren et al. do not disclose do not disclose receiving Doppler shift correction values from a data bus.

However, Koenck et al. discloses a high speed communication bus (Fig. 2, element 50) used to communication data between various modules in a data processing terminal (see column 15, lines 28-35). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to communicate data such as the Doppler shift correction value of Krasner Mendelovicz, and Warren et al. using a high-speed bus as disclosed by Koenck since Koenck states the high-speed bus (MBUS) provides reliability advantages (column 15, lines 28-35) and more compact physical routing of the cables between the modules (column 17, lines 42-44).

9. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krasner (previously cited in Office Action 4/21/2005) and in view of Mendelovicz (previously cited in Office Action 7/26/2006) and in further view of Warren et al. (previously cited in Office Action 7/26/2006) as applied to claim 39, and in further view of Furukawa et al. (previously cited in Office Action 7/26/2006).

Krasner, Mendelovicz, and Warren et al. disclose all the limitations of claim 42 including complex multiplying (mixing) the input signal with the Doppler frequency offset (shift) correction value (see Krasner, column 5, lines 28-50). Krasner, Mendelovicz, and Warren et al. do not disclose do not disclose receiving Doppler shift correction values from a lookup table.

However, Furukawa et al. discloses a coherent detection system which stores precomputed correction values (passbands) which compensate for Doppler shifts related to an input signal (see column 2, lines 50-63). The filter settings (passbands) are selected based on the Doppler shift in the signal. Therefore, it would have been obvious to store and receive precomputed correction values in the system of Krasner, Mendelovicz, and Warren et al. as taught by Furukawa et al. since Furukawa et al. states implementing these teachings can allow for demodulation of a signal even when a large Doppler shift occurs (column 2, lines 2-4).

Conclusion

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom
April 27, 2007

JAY K. PATEL
SUPERVISORY PATENT EXAMINER